Specifications for the MINOS MINDER Crate Backplane

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Preliminary

I. Introduction

This document describes the signals and the pin-out of the MINDER backplane. The J1 provides the digital signals needed to communicate between the MINDER and the KEEPER. The J2 provides signal feed-throughs for the phototube signals, in the signal transmission between the Auxilary cards in the rear of the crate, and the MINDERs (and KEEPER.) The J2 also distributes the power needed for the analog voltages.

II. J1 Backplane

1. Addressing: 12 bits

   MADD[11:0]

   Each Module shall have a set of 5 switches that sets it's slot address in the MINDER Crate. The slot address shall map into address space. (The slot address shall also determine which of the primary trigger signals a card responds to.) The address lines are sourced by the KEEPER.

2. Data: 16 bits

   MDATA[15:0]

   Used for general purpose I/O. The data lines on the backplane are bi-directional.

3. Data Strobes: 2 bits

   MSTB[1:0]

   Essentially 1 signal, OR'ed together on each card. Follows standard VME protocol. The signals are sourced by the KEEPER.

4. Data Bus Direction: 1 bit

   MWRITE*

   Determines the state of the data bus on the backplane. It is low-asserted (LOW = WRITE by KEEPER, HIGH = READ by KEEPER.) The signals are sourced by KEEPER.

5. Data Acknowledge: 1 bit

   MDTACK*

   This is the handshake between a MINDER and the KEEPER that a data transfer has been completed. It is low-asserted. The signal is sourced by the MINDERs using open collector outputs, and is wire-OR'ed on the KEEPER.

II. J1 Backplane (continued)

6. Address Enable: 1 bit

   MENBL*

   This is the enable to allow a card to be addressed. The signal is sourced by the KEEPER, and is low-asserted.

7. Crate-wide Reset: 1 bit

   MRESET*

   Used to reset certain registers on all MINDER Modules in the crate simultaneously (to be defined.) It is low-asserted. The signal is sourced by the KEEPER.

8. Control Bits: 8 bits

   MCTRL*[7:0]

   These are control lines used to set up conditions on all MINDER Modules in the crate simultaneously. (The functions are to be defined. Functions include normal data taking, current calibration, diagnostic data, etc.) The signals are sourced by the KEEPER, and are low-asserted.

9. Status Bits: 4 bit

   MSTAT*[3:0]

   These are status lines used to detect errors on the MINDER Modules. The signal MSTAT0* is reserved for use by the MINDER Timing Module (MTM.) The signals MSTAT1*, MSTAT2*, and MSTAT3* are for use by the MINDER Modules. (The functions are to be defined. Functions include transmission errors, clock sync errors, etc.) They are low-asserted. The signal are sourced by the MINDERs using open collector outputs, and are wire-OR'ed on the KEEPER. The KEEPER shall send MSTAT0* to the MASTER on a dedicated signal line. The KEEPER shall AND together MSTAT1*, MSTAT2, and MSTAT3*, and send the result to the MASTER on a dedicated signal line. The MINDERs will have to be queried to find the offending module.

II. J1 Backplane (continued)

10. Trigger Bits: 7 bits

MTRIG*[6:0]

These signals have several functions. MTRIG*[3:0] are the dynode trigger bits. The dynode signals are discriminated by the KEEPER, and the result sent out onto the MINDER backplane on dedicated signal lines. All four signals are received by all MINDER cards in the crate. A given MINDER Module shall be programmed as to which signal to process by the slot that it resides, and the position of it's address switches.

The signals MCTRL*[5:4] are for additional triggering functionality, and are not yet defined. One function shall be a global trigger, which causes all MINDER Modules to acquire data simultaneously, as needed in performing calibrations.

The signal MCTRL6* is reserved for use by the LED flashing system. When a trigger signal is received by the KEEPER, MCTRL6* is asserted after a fixed delay and for a fixed duration. Any dynode trigger generated during this gate shall be marked as a flash event.

The signals are sourced by the KEEPER, and are low-asserted.

11. Power: 3 pins of +5V Digital

Used for digital circuitry only.

12. Digital Ground: 7 pins of Digital Ground

Used for digital circuitry only.

Pin Number	Row A Signal Name	Row B Signal Name	Row C Signal Name
1	MDATA0	X	MDATA8
2	MDATA1	X	MDATA9
3	MDATA2	X	MDATA10
4	MDATA3	X	MDATA11
5	MDATA4	X	MDATA12
6	MDATA5	X	MDATA13
7	MDATA6	X	MDATA14
8	MDATA7	X	MDATA15
9	GND	X	GND
10	X	X	X
11	GND	X	X
12	MSTB1*	MSTAT0*	MRESET*
13	MSTB0*	MSTAT1*	X
14	MWRITE*	MSTAT2*	X
15	GND	MSTAT3*	X
16	MDACK*	X	X
17	GND	X	MCTRL7*
18	MENBL*	X	MCTRL6*
19	GND	X	MCTRL5*
20	X	GND	MCTRL4*
21	X	X	MCTRL3*
22	X	X	MCTRL2*
23	X	GND	MCTRL1*
24	MADD5	MTRIG6*	MCTRL0*
25	MADD4	MTRIG5*	MADD11
26	MADD3	MTRIG4*	MADD10
27	MADD2	MTRIG3*	MADD9
28	MADD1	MTRIG2*	MADD8
29	MADD0	MTRIG1*	MADD7
30	X	MTRIG0*	MADD6
31	X	X	X
32	+5V Digital	+5V Digital	+5V Digital

Table 1. J1/P1 Pin Assignments for the MINOS MINDER Crate Backplane

III. J2 Backplane

1. Power: 6 pins of +3.3V Digital

   VDIG1 is +3.3V

   Used for powering the MENU Modules only!

2. Power: 6 pins of +12V Analog

   VANA4 is +12V

   Used for analog circuitry only.

3. Power: 3 pins of +5V Analog

   VANA3 is +5V

   Used for analog circuitry only.

4. Power: 3 pins of -5V Analog

   VANA2 is -5V

   Used for analog circuitry only.

5. Power: 3 pins of -12V Analog

   VANA1 is -12V

   Used for analog circuitry only.

III. J2 Backplane (continued)

6. Precision Calibration Voltage: 1 pair of pins

   VCAL+, VCAL-

   This is differential calibration voltage used to calibrate the QIEs and trigger discriminators. It is sourced by a DAC on the KEEPER. The signals must be received differentially by all MINDER Modules, using a higg-impedance receiver.

7. PMT Input Signals - 16 pins

   Used to input PMT signals to the MINDER Modules.

8. PMT Return Signals - 37 pins

   Used to return the current pulses from the MENU Modules to the PMTs.

Pin Number	Row A Signal Name	Row B Signal Name	Row C Signal Name
1	AGND	AGND	AGND
2	MVDIG1	MVDIG1	MVDIG1
3	MVDIG1	MVDIG1	MVDIG1
4	AGND	AGND	AGND
5	MVANA4	MVANA4	MVANA4
6	MVANA4	MVANA4	MVANA4
7	AGND	AGND	AGND
8	MVANA3	MVANA3	MVANA3
9	AGND	AGND	AGND
10	MVANA2	MVANA2	MVANA2
11	AGND	AGND	AGND
12	MVANA1	MVANA1	MVANA1
13	AGND	AGND	AGND
14	AGND	VCAL-	AGND
15	RET	VCAL+	RET
16	RET	RET	PMT_SIG0
17	PMT_SIG1	RET	RET
18	RET	RET	PMT_SIG2
19	PMT_SIG3	RET	RET
20	RET	RET	PMT_SIG4
21	PMT_SIG5	RET	RET
22	RET	RET	PMT_SIG6
23	PMT_SIG7	RET	RET
24	RET	RET	PMT_SIG8
25	PMT_SIG9	RET	RET
26	RET	RET	PMT_SIG10
27	PMT_SIG11	RET	RET
28	RET	RET	PMT_SIG12
29	PMT_SIG13	RET	RET
30	RET	RET	PMT_SIG14
31	PMT_SIG15	RET	RET
32	RET	RET	RET

Table 2. J2/P2 Pin Assignments for the MINOS MINDER CrateBackplane